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Improvement on Semiconductor Substrate Design with Package Modeling and Simulation for Mitigation of Delamination and Voids

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Authors' contributions

This work was carried out in collaboration amongst both authors. Both authors read, reviewed, and approved the final manuscript.

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ABSTRACT

This technical paper presents the challenges encountered in the development of a compact and thinner package that incorporates multiple or stacked dice in one. For the case of this paper, Die1 (bottom die) is smaller than Die2 (top die) and must be the first one to be die-bonded, making the internal construction an unbalanced stacked dice. Typically, stacked dice are in pyramid layout, wherein a single large bottom die supports smaller top die. Nonetheless, success is measured when there is a solution to control or mitigate die-attach voids and eliminate or significantly minimise delamination for unbalanced stacked dice as mentioned. Ultimately, the paper presents the understanding of the factors involved and the package design optimisation approach used to produce a successful unbalanced stacked die in a thin package using a thin substrate.

Keywords: Substrate design; planarized; delamination; DAF voids; modeling; simulation.

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1. INTRODUCTION

The increasing interest to incorporate several dice into a single molded Integrated Circuit (IC) package to get multiple desired functions has led to the development of multiple dice or stacked dice configuration of semiconductor IC package. Instead of separately mounting electronic components like analogue ICs and digital ICs to the Printed Circuit Board (PCB), they can now be integrated into a single package.

In this study, the internal construction of the device (hereinafter referred to as Device Z) must be designed to stack smaller Die1 at the bottom and larger Die2 on top, as illustrated in Fig. 1 and 2. An interposer silicon die was added to support the top die overhang in Fig. 2. The stacked dice were supported by 0.13 mm substrate and molded with 0.42 mm mold cap.

Actual evaluation of the first version of Device Z, however, showed that there were issues of delamination between top and bottom dice, as well as die attach voids between bottom die and substrate. To resolve the issues encountered, factors involved in the delamination and voids were investigated and package design optimization focusing on substrate was carried out.

2. REVIEW OF RELATED LITERATURE

2.1 Stacked Dice Using DAF on Substrates

For stacked dice configuration, the die attach material normally used is the Die Attach Film (DAF). Currently, DAF is being widely applied on various high density packages such as Ball Grid Array (BGA), Chip-Scale Package (CSP), System-In-Package (SIP), Package on Package (PoP) and so on due to its bleedless and consistent Bond Line Thickness (BLT) [1,2,3]. Typical assembly flow of BGAs includes dicing die attach film (DDAF), which integrates the die attach film and the dicing tape [1,4,5]. Conventional assembly flow with the liquid-type die-attach material can be easily applied to packaging with DAF. The process could be simplified by eliminating the dispensing and also skipping the post die to attach cure. However, DAF void always is one of the major concerns, especially for its application between the die and the substrate [6,7]. Reliability issue of delamination likely occurs at the DAF-substrate interface [6,8]. DAF void characteristics and its formation and reduction mechanism were then studied. Aside from die attach or diebonding parameters, many other factors are inevitable with regards to the void performance. For Device Z, DAF voids between bottom dice (Die1 and interposer) and substrate were also considered as one of the contributors for the Die2 (top die) delamination issue.

2.2 Substrate Package Design Layout

The substrate is normally constructed with metal planes to ensure Copper (Cu) balance and solder mask balance between layers to ensure no substrate delamination when subjected to reflow [8]. Electrical simulations in relation to the metal plane or metal strips in substrate should govern for resistance, inductance and capacitance. Fig. 3 shows the 2 layer (top side – M1 and bottom side - M2) construction of the substrate for Device Z, with the metal balance of 16%.

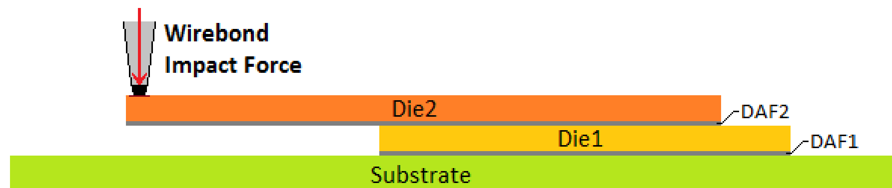


Fig. 1. Cross-section of unbalanced stacked dice, affecting wire-bonding process

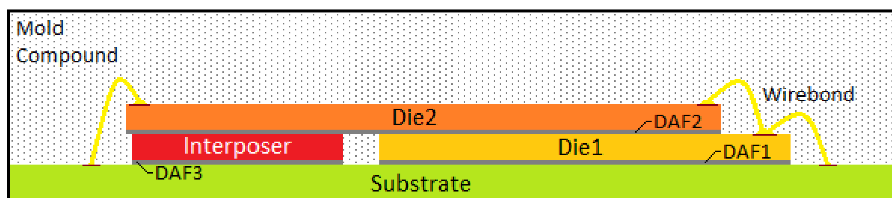


Fig. 2. Package cross-section with added interposer to support the Die2 overhang

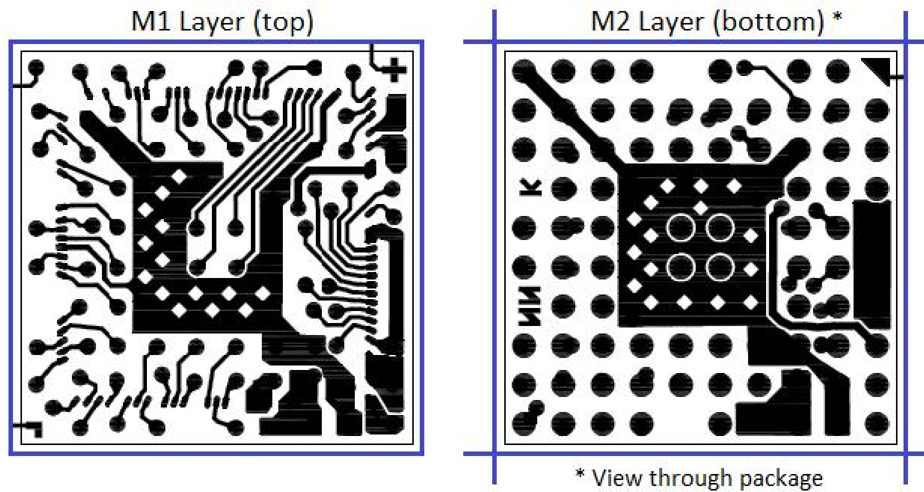


Fig. 3. Substrate design layout top and bottom view

3. METHODOLOGY

3.1 Design Modification and Modeling

The first version of the Device Z design created was using rigid and thin DAF with 20 μm thickness for all stacked dice to ensure planarity in-between interfaces – 2 bottom dice to the substrate and top die to the 2 bottom dice, and to ensure there is enough clearance for the wire bonds looping after mold. Back-end assembly of Device Z was performed from die preparation to package singulation and submitted samples for Moisture Sensitivity Level 3 (MSL3) to check for delamination. Reliability test showed top die delaminated from bottom dice and observed presence of DAF voids after cross-section validation. Fig. 4-5 shows the MSL3 results.

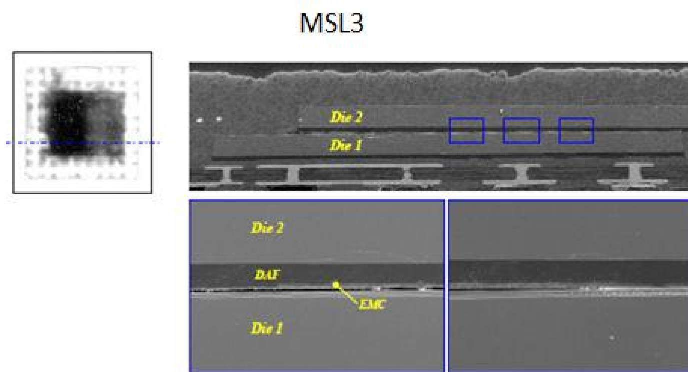


Fig. 4. Delamination at Die2 (top die)

Fig. 5. DAF voids at Die1 (bottom die)

With the results, a fault-tree analysis in Fig. 6 was then performed to prove the phenomenon that the ground plane expands after heat is applied.

3.2 Correlation between DAF Voids and Substrate Topology

With the occurrence of voids between substrate and DAF interface with fixed pattern, affecting Die2 (top die) to delaminate, the substrate topography is mostly suspected. Fig. 7 shows that to identify the correlation between void and substrate surface, the cross section was further analyzed and found out that the metal plane expansion serves as fulcrum (not only as source of voids) thus affecting the planarity of 2 bottom dice which resulted to top die aggravated delamination. Therefore, the ground metal plane serves as peaks and solder mask as valleys.

It can be observed that in every after metal plane, there is large void between die and substrate. Measurements of the peaks and valley were more than 10 µm and DAF thickness is at 20 µm. With this, DAF needs to fill the gap with depth equivalent with 50% of its thickness, which produces the challenge towards DAF gap filling capability. Therefore, these voids result from the insufficient gap and it can be explained that DAF voids have the properties of fixed position and similar pattern, which is matched with substrate surface topography.

A comparison of the original or non-planarized substrate and the planarized substrate was performed to check the difference as shown in Fig. 8. Difference of more than 5 microns was observed.

Fig. 6. Fault-tree analysis

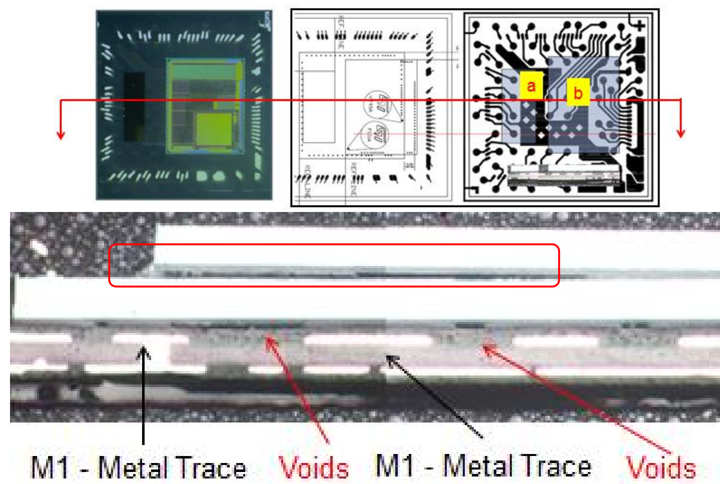
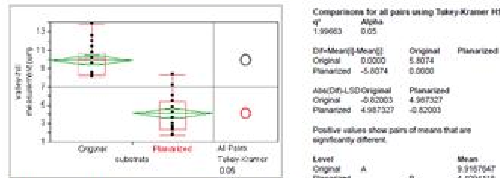


Fig. 7. Metal trace of ground plane served as fulcrum and induced voids, thus top die delamination encountered

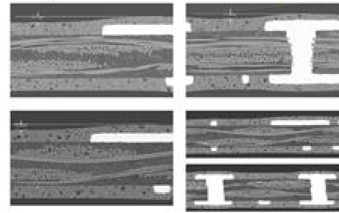
	Original	Planarized
Minimum	8.02 um	1.75 um
Average	9.92 um	4.11 um
Maximum	13.70 um	8.33 um
StDev	1.564 um	1.814 um

Planarity measurements are vertical depths from highest plateau points relative to lowest valley point.



Statistically, significant difference is exhibited between the original/non-planarized and the planarized substrate.

Original/Non-Planarized Substrate



Planarized Substrate

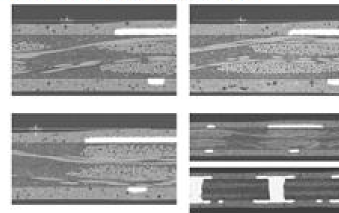


Fig. 8. Non-Planarized vs. Planarized comparison

Table 1. Process evaluation matrix

Evaluation Run #	DAF Evaluation	Substrate (with variation)	Remarks
1	Top die and Bottom dice – rigid and thin (20 µm)	Non-planarized – existing for Device Z	Control Run: Samples should fail MSL3 to validate the issue (with cross section validation)
2	Top die – softer and Thicker DAF (30 µm), Bottom dice – rigid and thin (20 µm)	Non-planarized – existing for Device Z	Samples must pass MSL3 with cross section validation
3	Top die – softer and Thicker DAF (30 µm), Bottom dice – rigid and thin (20 µm)	Planarized from another package	Response in time (0) with cross-section validation

3.3 Design Iterations

Considering the findings from the fault-tree analysis in Fig. 6, up to the cross-section verification in Fig. 7, the root cause of Die2 (top die) delamination and voids between bottom dice and substrate is the substrate topography. Softer and thicker DAF for Die2 was considered to compensate variation of level of the two bottom dice (Die1 and interposer). Table 1 was considered to further validate the hypothesis using the existing materials in the production line.

4. DISCUSSION OF RESULTS

Simulation results based on thermo-mechanical package modelling in Fig. 9 showed that warpage is relatively low. Actual package observation also confirmed the predicted low package warpage. Interface stress due to the Coefficient of Thermal Expansion (CTE) mismatch is also low, which implies that delamination could be due to other factors. Results of the package modelling exhibited low risk if DAF material adhesion is high.

Reliability tests (MSL3) were done using a different DAF, this time softer and thicker DAF for Die2 (top die). Shown in Figs. 10 and 11 are the MSL3 results.

Results of the evaluation are summarised in Table 2. Based on the results, Die2 (top die) should use softer and thicker DAF while bottom dice (Die1 and interposer) should use rigid and thinner DAF on a planarized substrate.

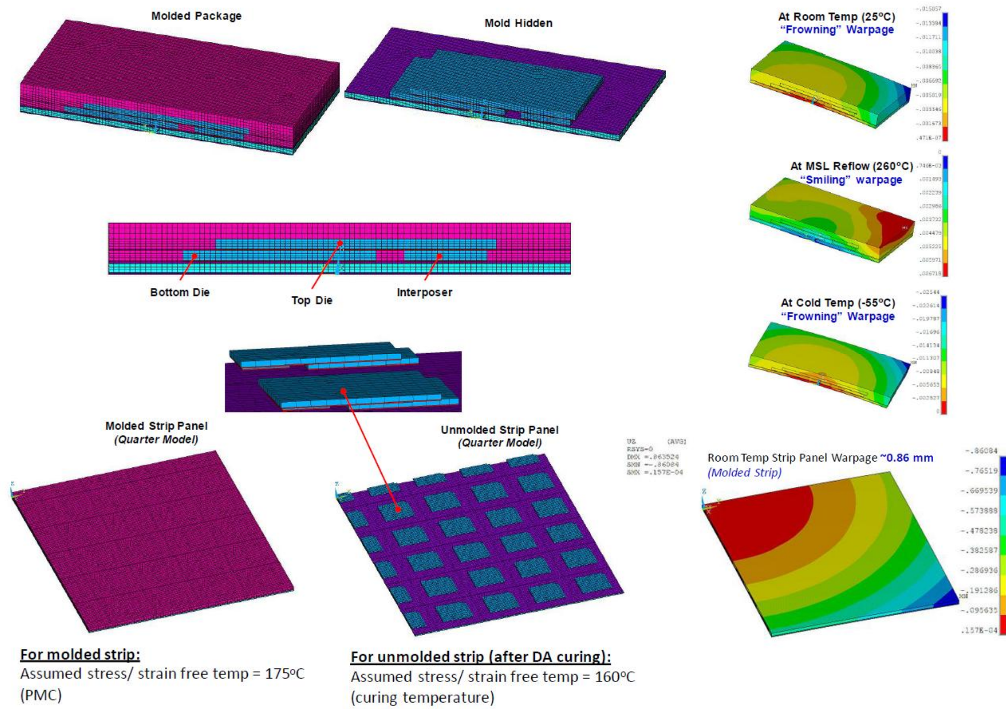


Fig. 9. Device Z thermo-mechanical simulations - package level and strip level

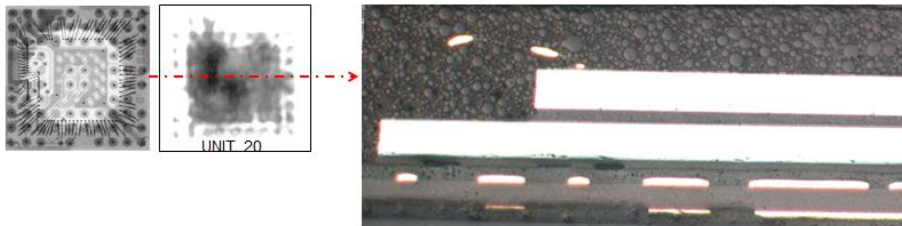


Fig. 10. MSL3 passed on assembly package performed using softer and thicker DAF for Die2 (top die)

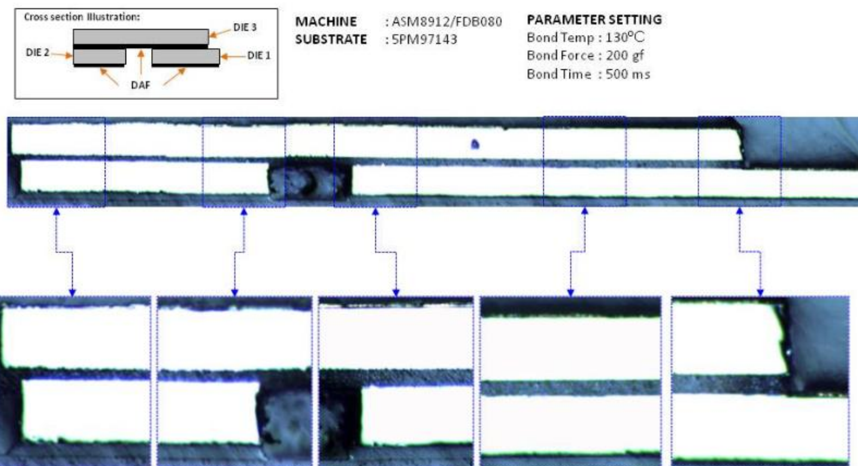


Fig. 11. Die attach stacked die using same rigid and thin DAF showed zero (0) voids for bottom dice at time zero (0)

2-Layer, 0.13mm	M1: Top Layer	M2: Bottom Layer	Cu Balance
Non-Planarized (Original design)			16%
Planarized (New design, Cu metal plane changed to metal strips)			6% (better)

Fig. 12. Proposed planarized substrate – metal strip design

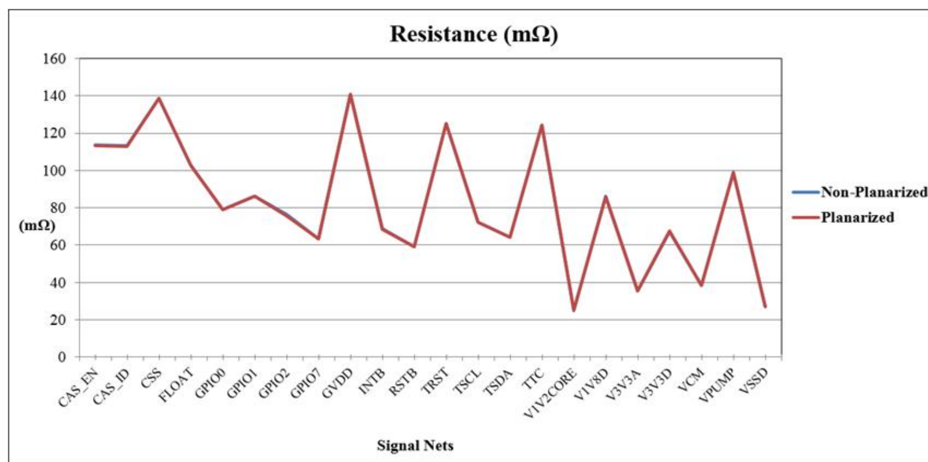


Fig. 13. Resistance comparison of signal nets of 2 designs

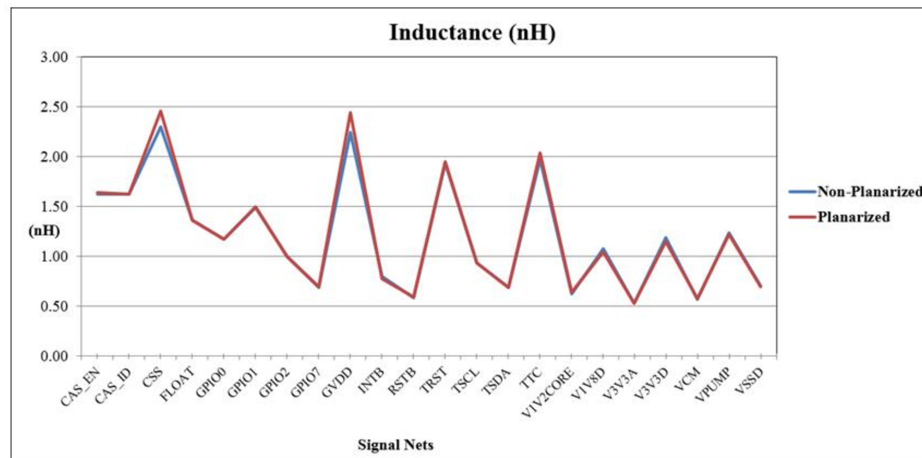


Fig. 14. Inductance comparison of signal nets of 2 designs

Table 2. Summary of evaluation results

Evaluation Run #	Results	Remarks
1	Fail	Previous issue replicated
2	Pass	Passed MSL3
3	Pass	Passed die attach responses

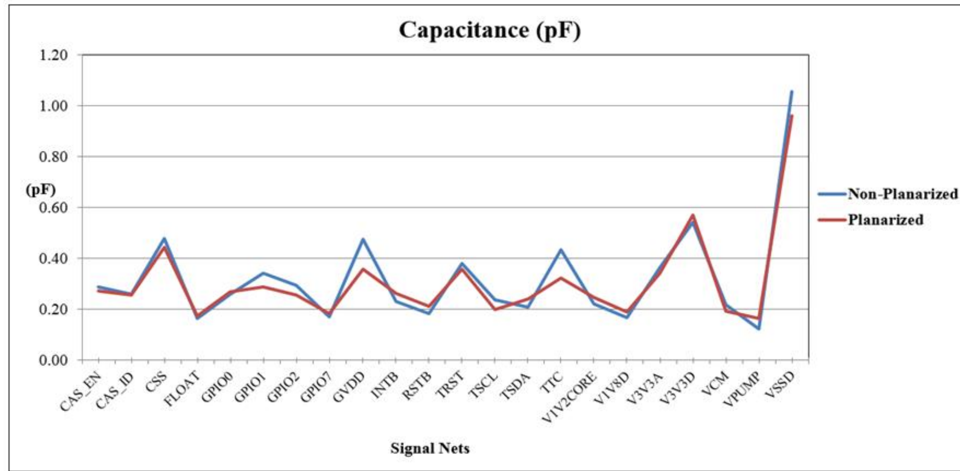


Fig. 15. Capacitance comparison of signal nets of 2 designs

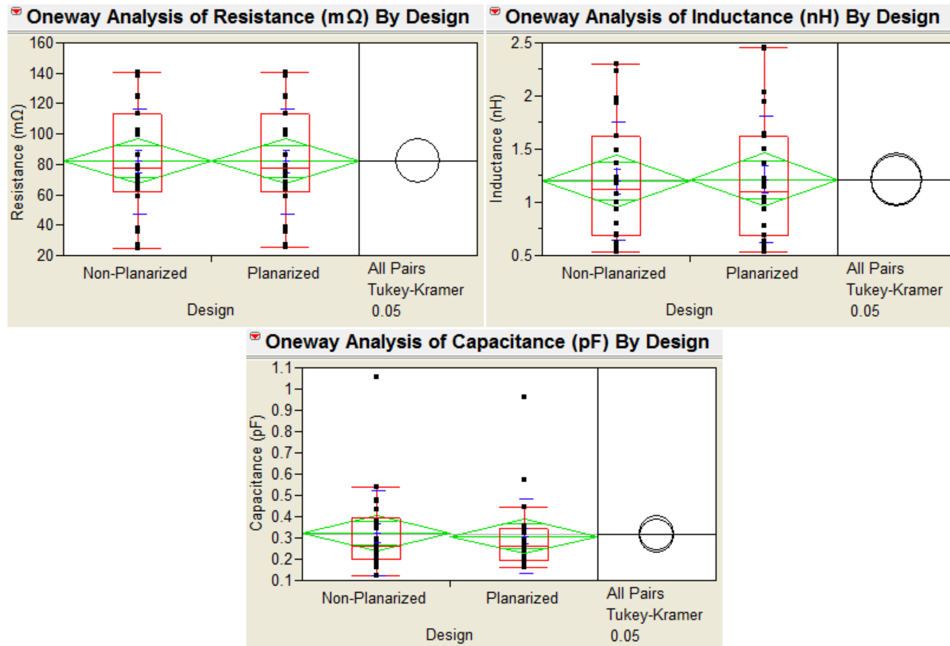


Fig. 16. Statistical analysis graphs showing no significant difference in resistance, inductance, and capacitance of signal nets between the 2 designs

5. CONCLUSIONS AND RECOMMENDATIONS

Based on the study with the three evaluation runs completed, the planarized substrate should be considered for DAF application. Die2 (top die) should use softer and thicker DAF to compensate the variation of bottom dice. On the other hand, bottom dice (Die1 and interposer) should use rigid and thinner DAF to maintain level.

New substrate design for Device Z proposal is shown in Fig. 12, replacing the metal plane in M1 with strip type metals and reducing M2 density resulted to better Cu balance [9]. Figs. 13-16 showed no significant difference in package electrical modelling performance for resistance, self-inductance and self-capacitance.

Based on the results, it is highly recommended to optimise DAF selection and substrate design when developing stacked die. Since this study

has just focused on substrate design to eliminate delamination and voids, it is also recommended that DAF selection should be considered to ensure robustness of material selection.

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DISCLAIMER

Some part of this paper was previously presented in the following symposium with the following title:
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Title: Elimination of Voids and Delamination in Unbalanced Stacked Dice by Optimizing Substrate Design
Available:https://docplayer.net/56266617-23-rd-asemep-national-technical-symposium.html, https://jefftalledo.files.wordpress.com/2016/03/elimination-of-voids-and-delamination-by-optimizing-substrate-design.pdf

COMPETING INTERESTS

Authors have declared that no competing interests exist.

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